Modes of DMA:

The 3 data transfer modes of DMAC are :-

1.) Single Transfer Mode
2.) Block Transfer Mode
3.) Demand or Burst Transfer Mode

1.) Single Transfer Mode :- In this, device can make only one transfer (byte or word).
After each transfer DMAC gives the control of all buses to the processor. Due to this, processor can have access to the buses on a regular basis.
It allows the DMAC to time share the buses with the processor, hence this mode is most commonly used.

Way of doing the operation in this mode :-

a.) I/o device asserts DRQ [when it is ready to transfer data]
b.) DMAC asserts DREQ [to request use of buses from MP]
c.) MP asserts HLDA [granting control of buses to DMAC]
d.) DMAC asserts $\overline{DACK}$ [requesting I/o device to transfer data]
e.) I/o device deasserts its DREQ [after transfer of 1B/word]
f.) DMA deasserts $\overline{DACK}$ line
g.) Word/Byte transfer count is decremented and the memory address is incremented.
h.) HOLD line is deasserted to give control of buses back to MP.
i.) Same process is then repeated until last transfer.

2.) Block Transfer Mode :- In this mode, device can make no. of transfers as programmed in the word count register. After each transfer, word count (WC) is decremented by 1 and the address is decremented / incremented by 1.
The DMA transfer count is continued until the WC 'rolls over' from 0000 to FFFFH, a terminal count (TC) or an external 'end of process' ($\overline{EOP}$) is encountered.
This mode is used when DMAC needs to transfer a block of data.

Way of doing the operation in this mode :-

a.) same
b.) same
c.) same
d.) same
e.) same
f.) same
g.) same
h.) same
i.) When TC is not exhausted, the data transfer is not complete and the DMAC waits for another DMA request from I/O device.
j.) If TC is exhausted, DMA relinquishes control of buses to the processor.

③ Demand or Burst Transfer Mode :- In the mode, the device is programmed to continue making transfers until a TC or $\overline{EOP}$ is encountered or until DREQ goes inactive.

Way of doing the operation in this mode :-

a) same

b) same

c) same

d) same

e) same

f) same

g) same

h) same

i) If further demand is there [TC is not exhausted] I/O device transfers next byte of data.

j) If demand ceases, DMA relinquishes control of buses to µP.